Minute Meetings 2/1/2016 NG Sponsor Call

Discussed admin information. Get the website done by Wednesday, the 3rd. Talked with ME’s on the component box, will meet Friday the 5th at 10 am. Reimbursement issues have been pseudo-solved.

Olivier, take your notes, figures and pictures. Start laying out for the presentation slides. The multimeter display demo on the VGA is working with varying levels of voltage from a power supply. This gets us familiar with how to talk to display for sending data to display to show energy levels in scene. Implement the logic cell to display the negative voltage values coming from the negative side of the IQ demodulator.

MATLAB fast fourier transform demo is about 40% complete. Will be done in coordination with Olivier on the FPGA logic core by Wednesday, to show the FFT can be done on either the FPGA or MATLAB.

Component housing. Parts must be ordered by weekend after Presentation I, have shopping cart full and ready to order, can be tweaked if any criticism is given during the presentation, but will be ordered that following weekend, on the 19th or 20th.

State diagram is being prepared to be worked on. Has not been completed yet, but can be worked on and Scott and Jordan can help Olivier. Realistically, can be worked on by Friday night. Something will be done by then, the 5th. Deadline would be Monday the 8th. (For top-level state diagram of finite state machine that runs everything. Probably just up to the switching.)

Delay line test. 40 dBm power loss. This simulates the path loss through free space. We will probably attenuate this a little bit further. This sounds like a good value. It would be reasonable to start running the delay line test, or at least try to do this by the time Pete gets here. We can test this in the old component box. Test using the manual switching controls. Will have to order new adapters, or check to see if we already have them. There are a lot of attenuators in the spare parts. We have 50-Ohm terminators, which will greatly help.

Signal path verification would be unrealistic to have 100% complete by Presentation I, but can be done by the end of the month before the March NG visit. Get some separate parts of the signal paths verified at least, but there is no reason to be criticized on it because this was done last year and we are to be working on new tasks. If there is a problem, we can fix it because we have spare parts.

Talk with Kacey about the NG trip. We know they are coming, but who is coming and when is not too clear. March 2nd is something to do with outside of the project, but not a guarantee. Pete will check on his end for clarification on what exactly will happen. All we know is that one of the VPs is an alumni of the college, and apparently is coming for a technical presentation. How accurate this is may be an issue.

Mike will be coming at the same time as Pete, because hardware will actually be on hand, this will be an ideal scenario to have things synched up between both the electrical and mechanical teams.

We would like to have the control lines run to the switches so that we can do out electrical testing in a much more efficient manner. The first stage is so have the pins in the channel, verify that acceptable voltage is being applied, connect these to switches, and verify it switches, then test it in the component box. Make sure the slider switches are commanding the particular output that we want. Try to find my soldering iron next time I visit home, would be nice for final connection of switches to pins. Not too time sensitive.

We need to take a closer look at the VCO to see how far we are from getting this up and running. We can get an assessment to see how far we are from having it being operational. Can do the assessment on Friday the 5th.

Probably will not be ready for full scale testing by early March for actual RF testing. Start thinking about dates for this, follow up with Dr Foo about finding a test room. Connect transmit to receive, and show that as we change the phase, (get a phase shifter to put in delay line path, emulates making delay line path longer or shorter), the I and Q values change. As phase changes, then then the I and Q values change and map out a circle in the polar plane to prove that the RF is working.

What happened with the bad switch? We do think it is bad, it isn’t switching. We need to verify that it isn’t splitting. Will test a good switch for verification purposes before we send off the faulty switch. Good learning experience to find out and report on what exactly caused the problem. Good engineering practice.

How to create bin files from MATLAB and how to transfer these over to the FPGA using ADEPT. Find out how to get memory from the memory test. There can be a bug that shows up when you pull the memory off of the FPGA. Can load .bin files onto the memory. We can fill up the memory with the basis functions. Create all of these basis function in matlab, create them as a signed binary file, then load them in memory. When the data comes up to the A/D, then we can do some complex multiplication. If we don’t put basis functions into the memory, if we just take the data from the A/D and do processing in MATLAB, put data into the SRAM. This requires being able to talk to the SRAM of the FPGA. If we can use slider switches to switch between different paths, then depending on the path, we can send I and Q values to memory, then using Adept, send these values to MATLAB to verify the signal processing. Try to get this as much of a real time processing as possible. Do incremental demos for each step.